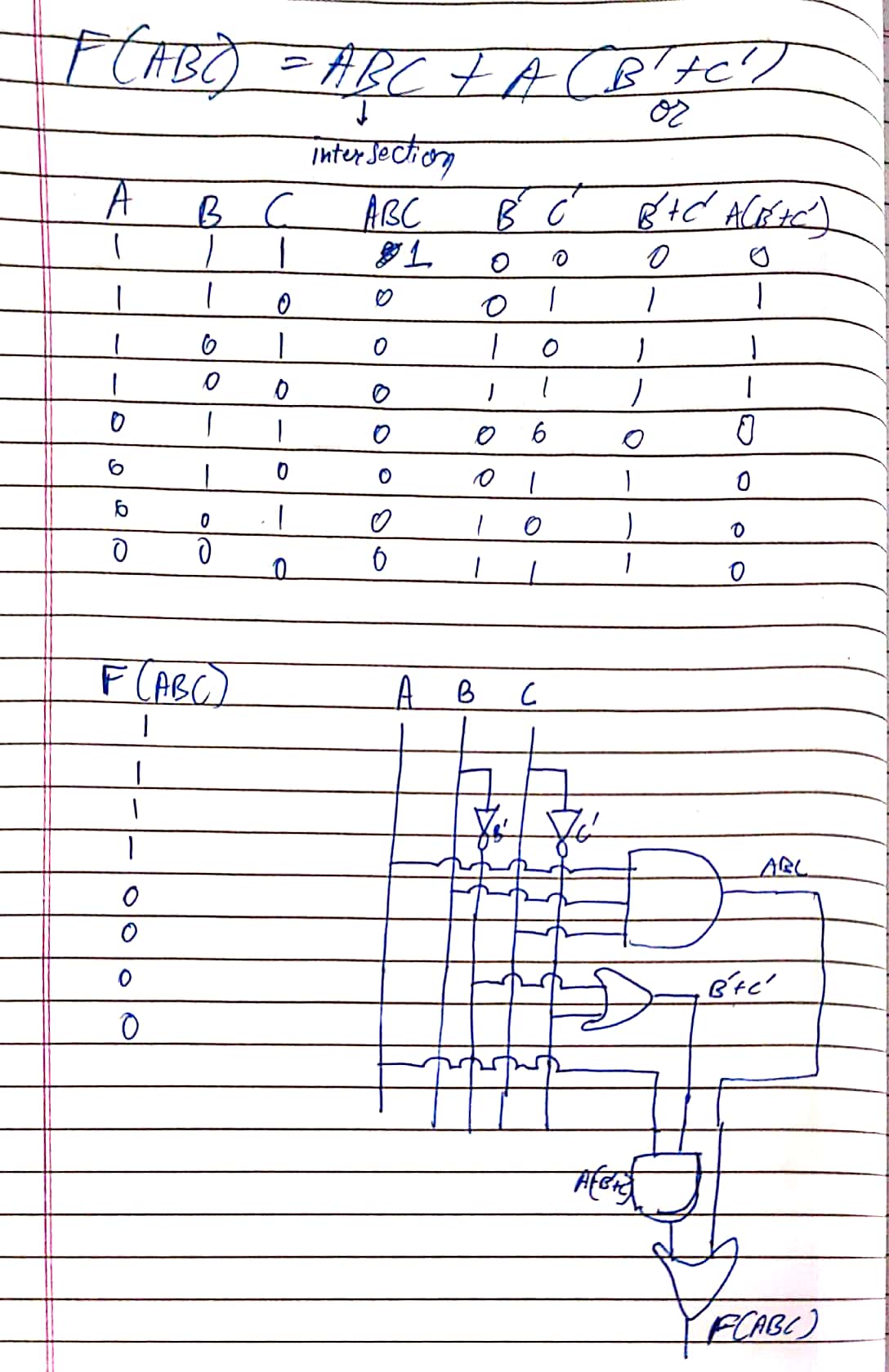
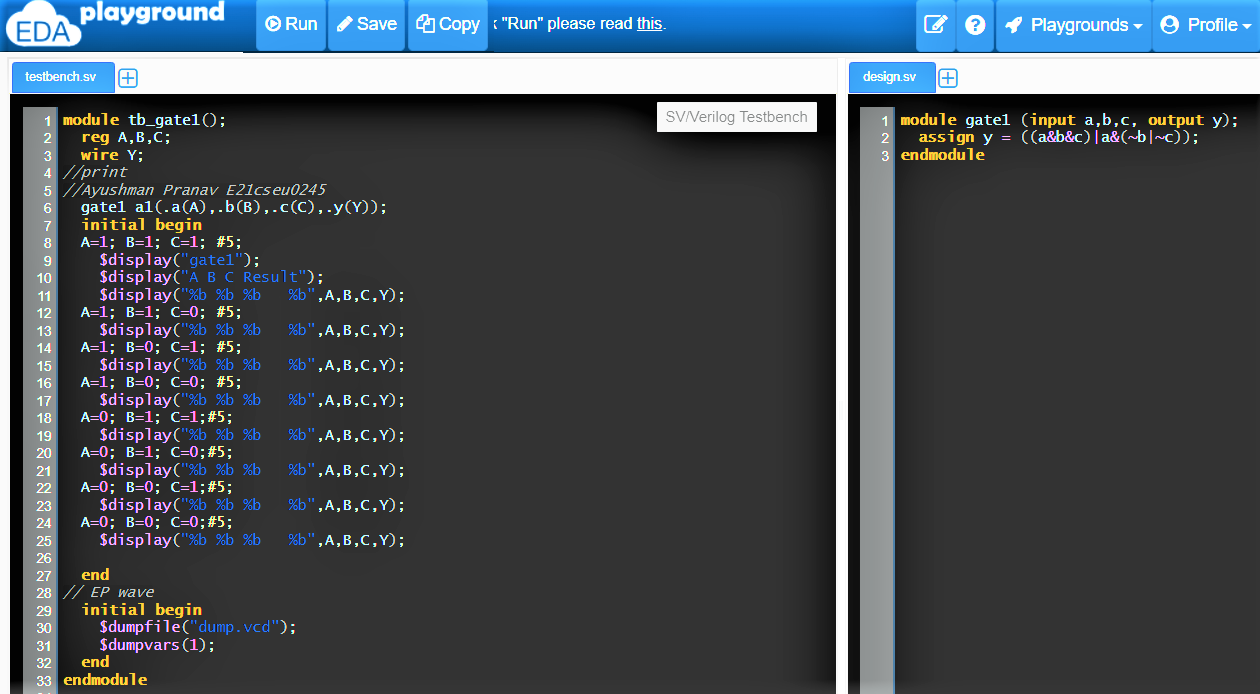
Lab Assignment 3

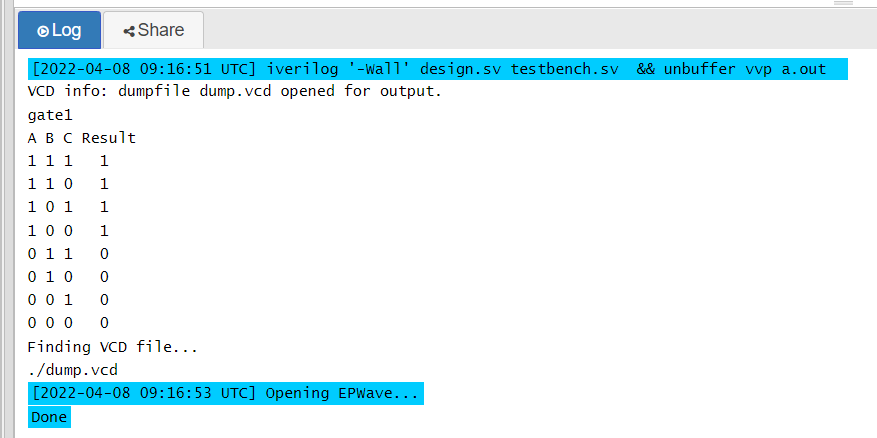
1. Perform the following operation on a given Boolean expression:

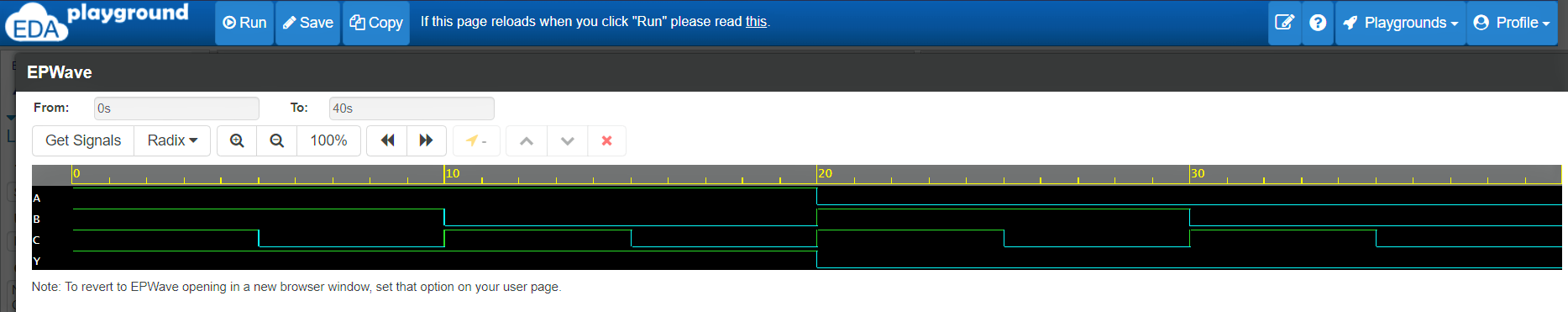
F(ABC) = ABC + A (B’ + C’)

* 1. Write a truth table for each Boolean expression.
  2. Draw a schematic diagram for each Boolean expression.
  3. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?









**Design bench.sv**

module gate1 (input a,b,c, output y);

assign y = ((a&b&c)|a&(~b|~c));

endmodule

**Test bench.sv**

module tb\_gate1();

reg A,B,C;

wire Y;

//print

//Ayushman Pranav E21cseu0245

gate1 a1(.a(A),.b(B),.c(C),.y(Y));

initial begin

A=1; B=1; C=1; #5;

$display("gate1");

$display("A B C Result");

$display("%b %b %b %b",A,B,C,Y);

A=1; B=1; C=0; #5;

$display("%b %b %b %b",A,B,C,Y);

A=1; B=0; C=1; #5;

$display("%b %b %b %b",A,B,C,Y);

A=1; B=0; C=0; #5;

$display("%b %b %b %b",A,B,C,Y);

A=0; B=1; C=1;#5;

$display("%b %b %b %b",A,B,C,Y);

A=0; B=1; C=0;#5;

$display("%b %b %b %b",A,B,C,Y);

A=0; B=0; C=1;#5;

$display("%b %b %b %b",A,B,C,Y);

A=0; B=0; C=0;#5;

$display("%b %b %b %b",A,B,C,Y);

end

// EP wave

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

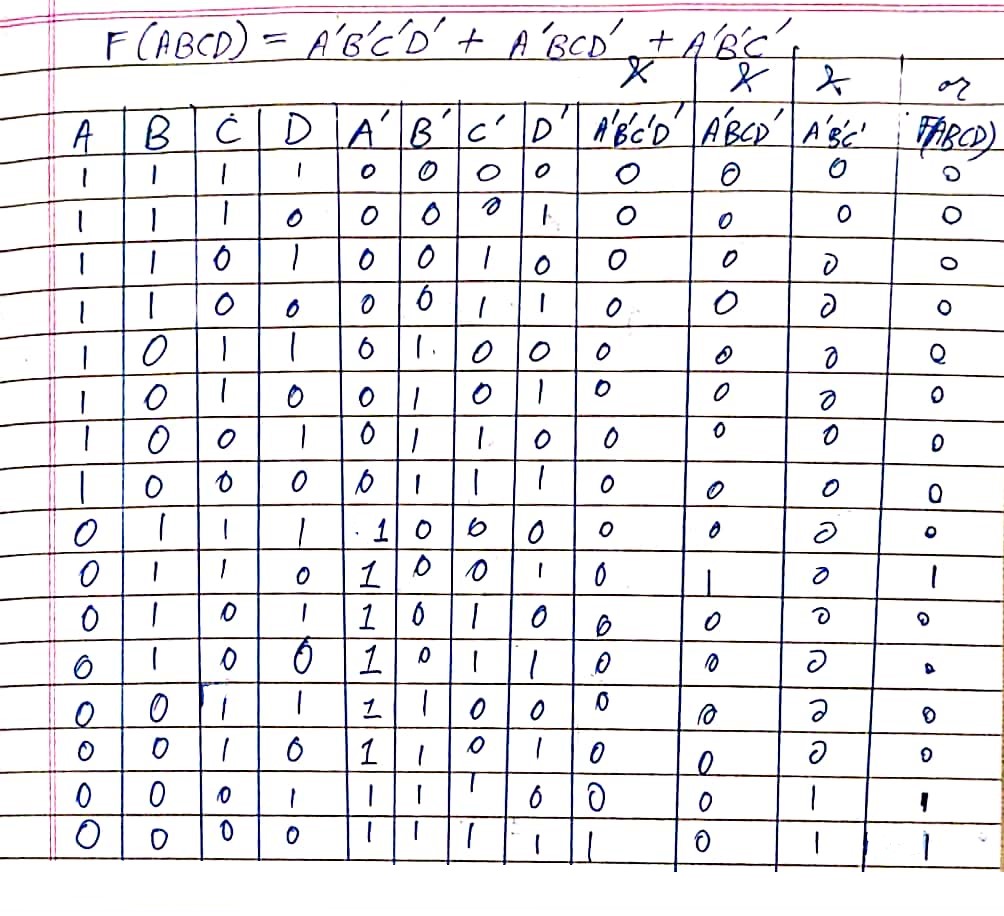
end

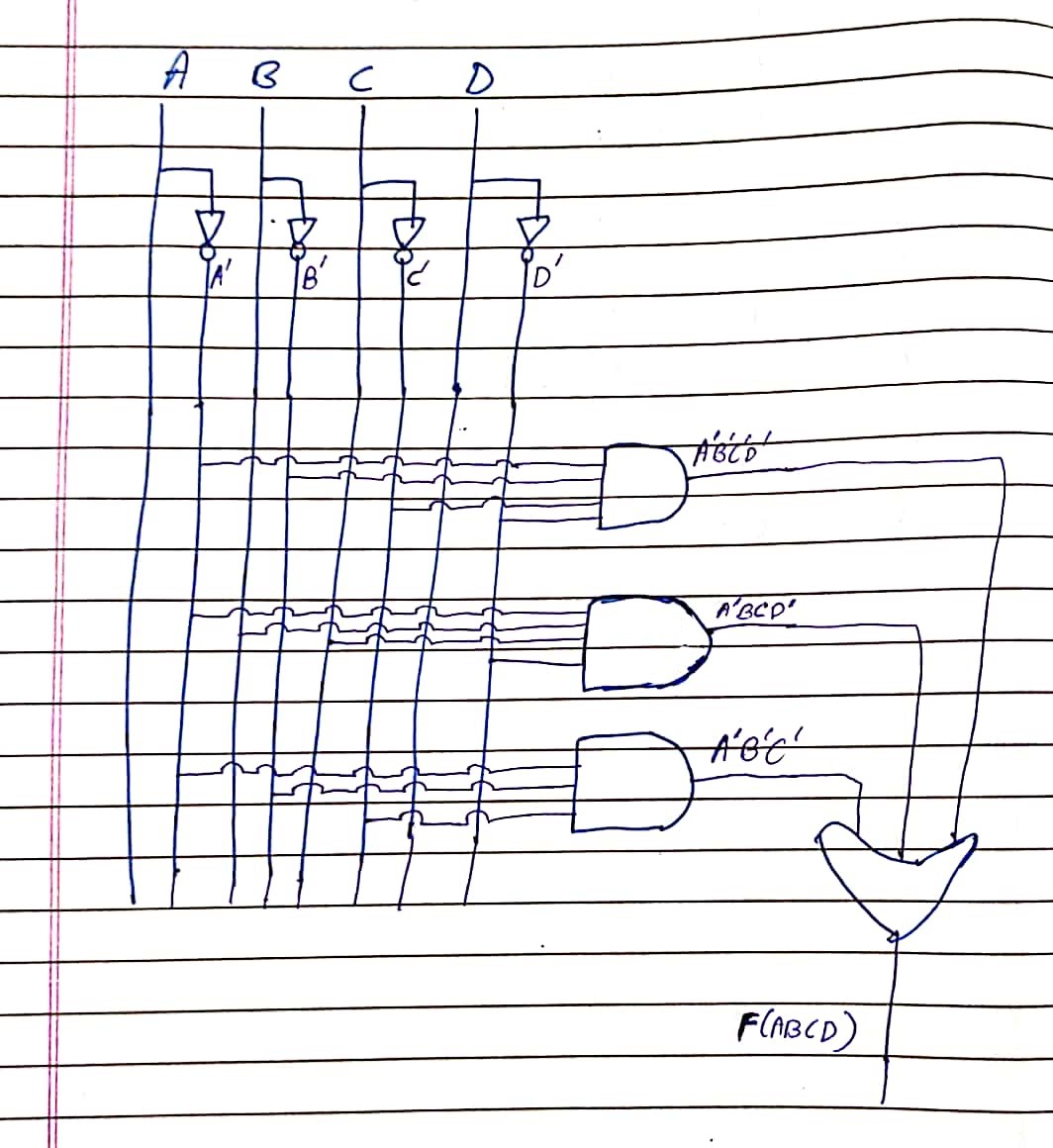
endmodule

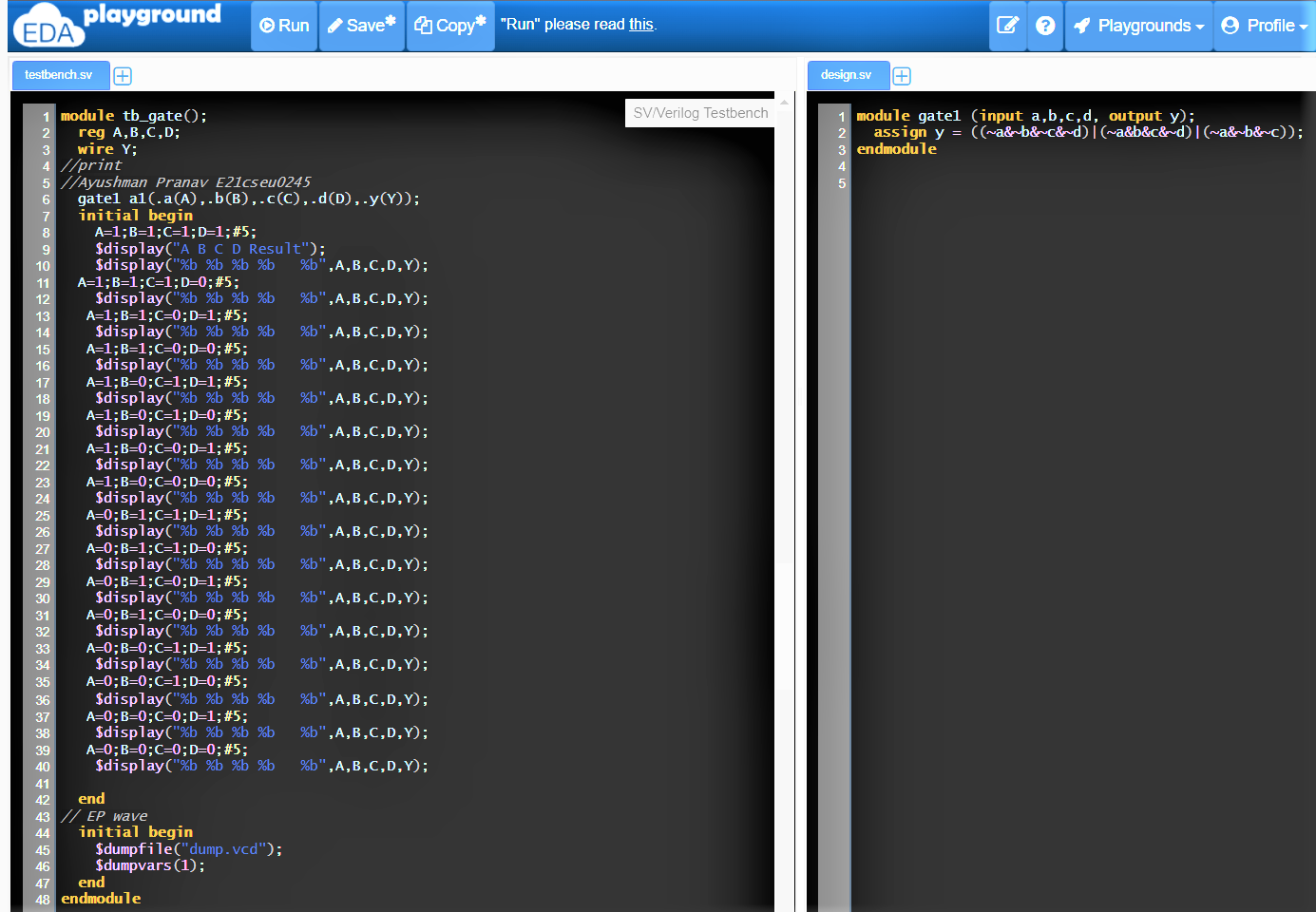
1. Perform the following operation on a given Boolean expression:

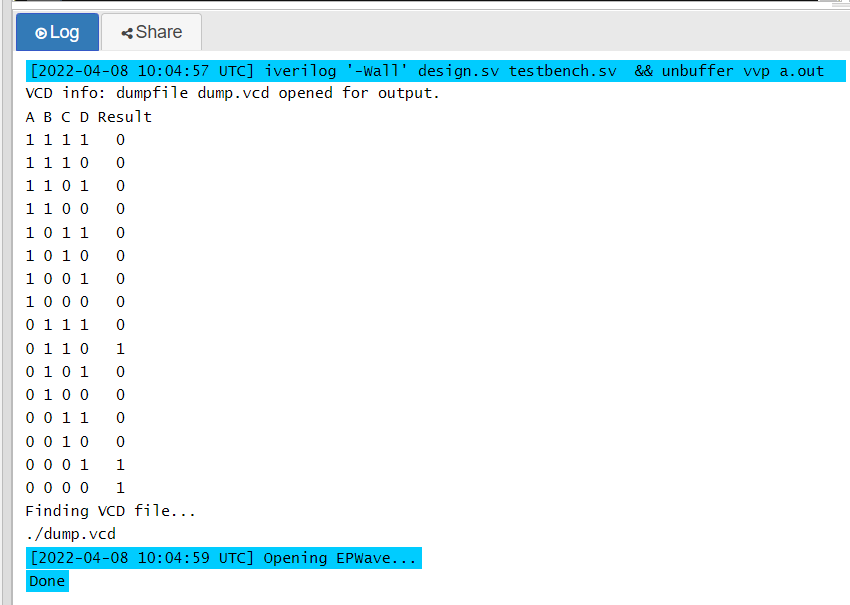
F(ABCD) = A’B’C’D’ + A’BCD’ + A’B’C’

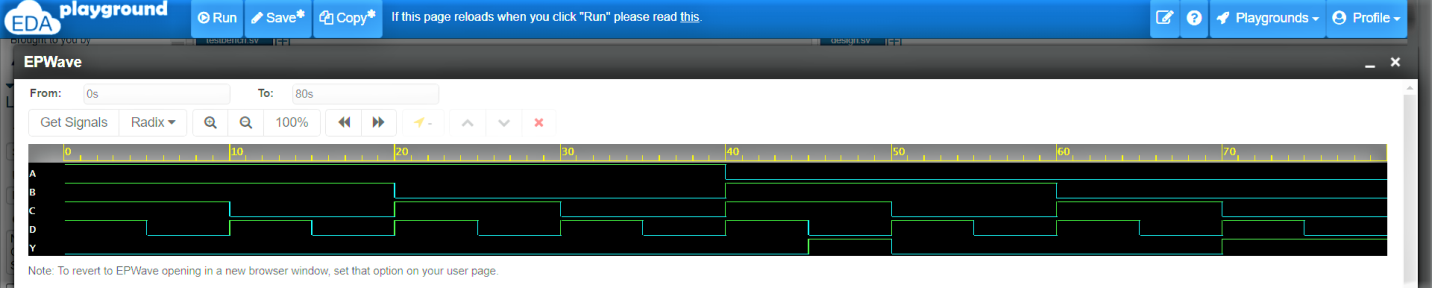
* 1. Write a truth table for each Boolean expression.
  2. Draw a schematic diagram for each Boolean expression.
  3. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?











**Design bench.sv**

module gate1 (input a,b,c,d, output y);

assign y = ((~a&~b&~c&~d)|(~a&b&c&~d)|(~a&~b&~c));

endmodule

**Test bench.sv**

module tb\_gate();

reg A,B,C,D;

wire Y;

//print

//Ayushman Pranav E21cseu0245

gate1 a1(.a(A),.b(B),.c(C),.d(D),.y(Y));

initial begin

A=1;B=1;C=1;D=1;#5;

$display("A B C D Result");

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=1;C=1;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=1;C=0;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=1;C=0;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=0;C=1;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=0;C=1;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=0;C=0;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=1;B=0;C=0;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=1;C=1;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=1;C=1;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=1;C=0;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=1;C=0;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=0;C=1;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=0;C=1;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=0;C=0;D=1;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

A=0;B=0;C=0;D=0;#5;

$display("%b %b %b %b %b",A,B,C,D,Y);

end

// EP wave

initial begin

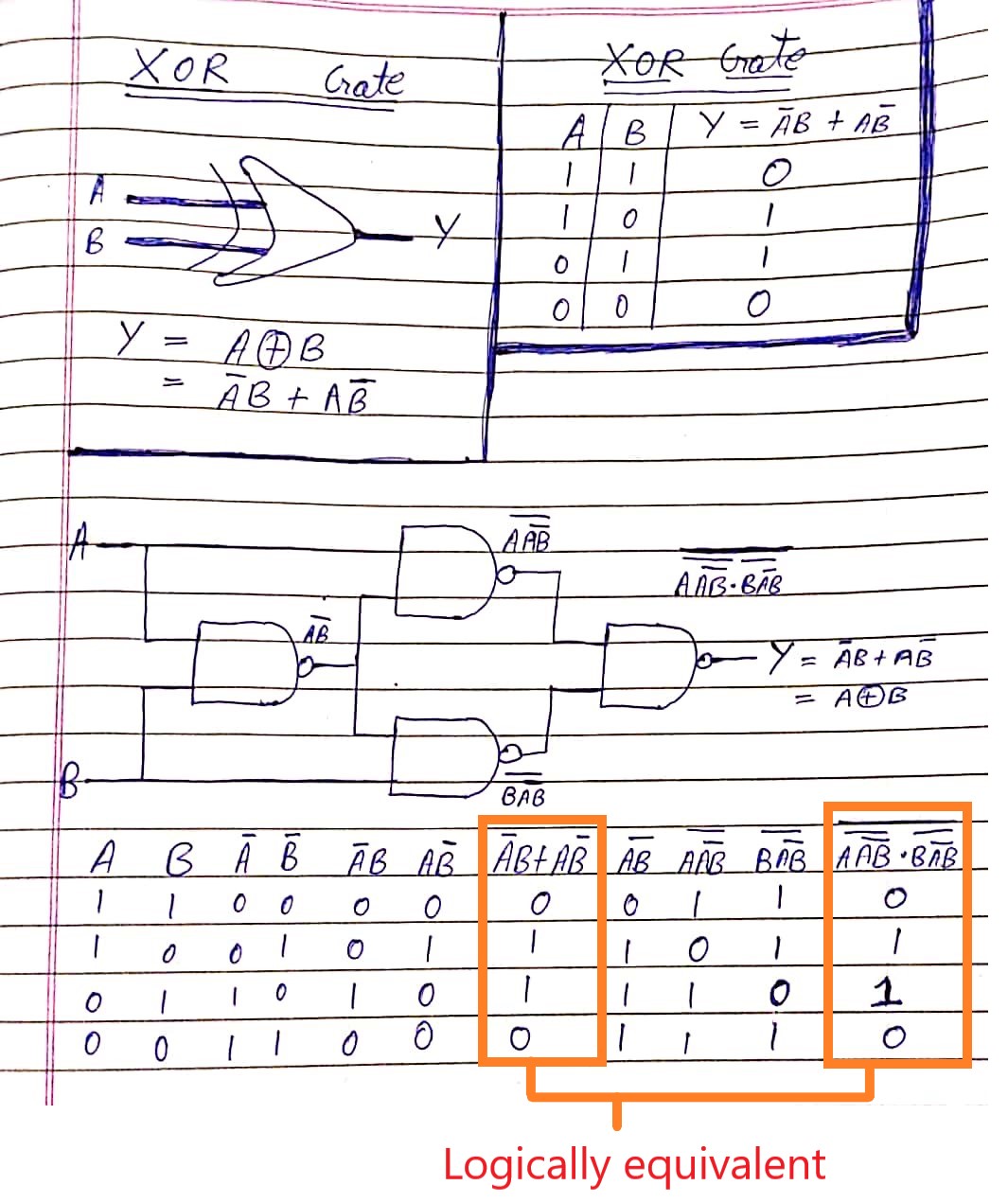
$dumpfile("dump.vcd");

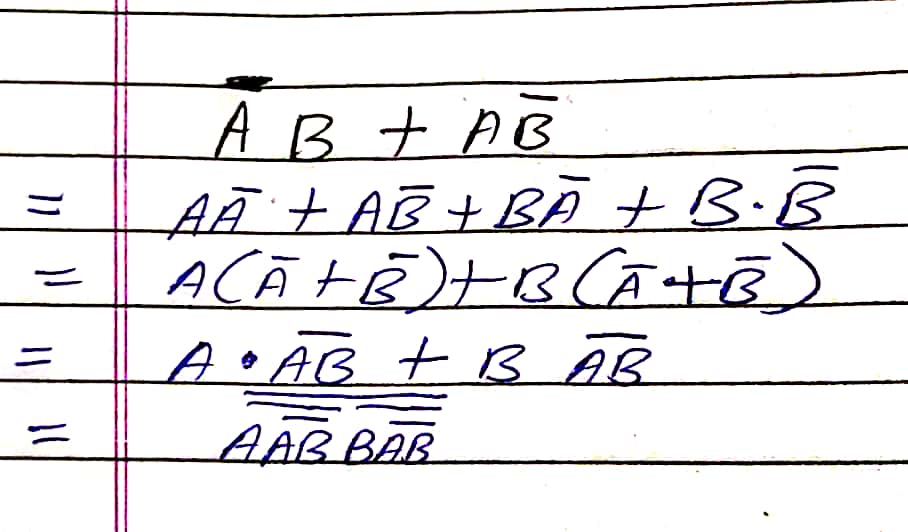
$dumpvars(1);

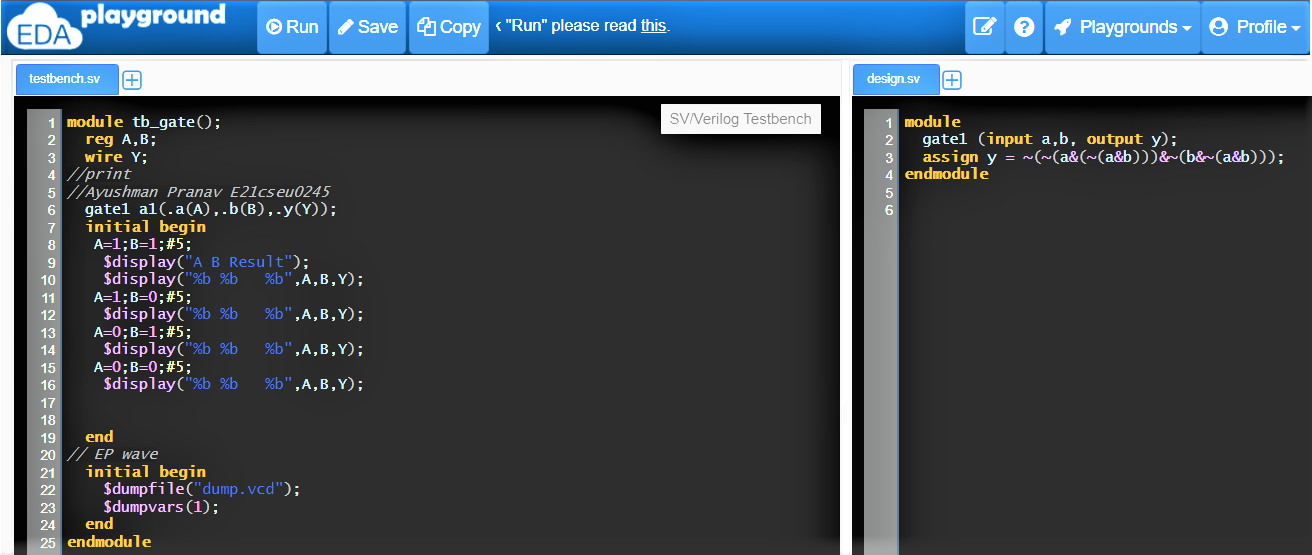
end

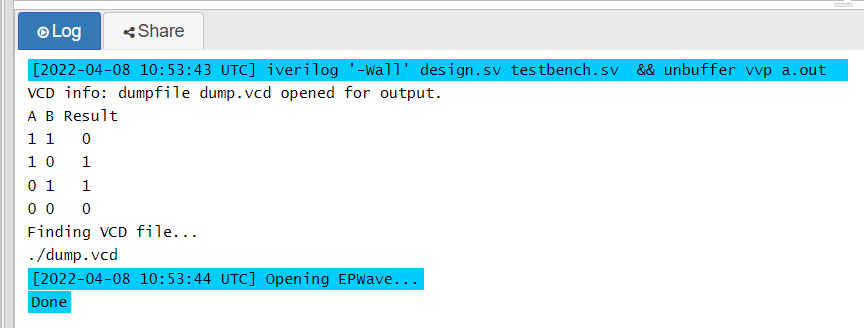
endmodule

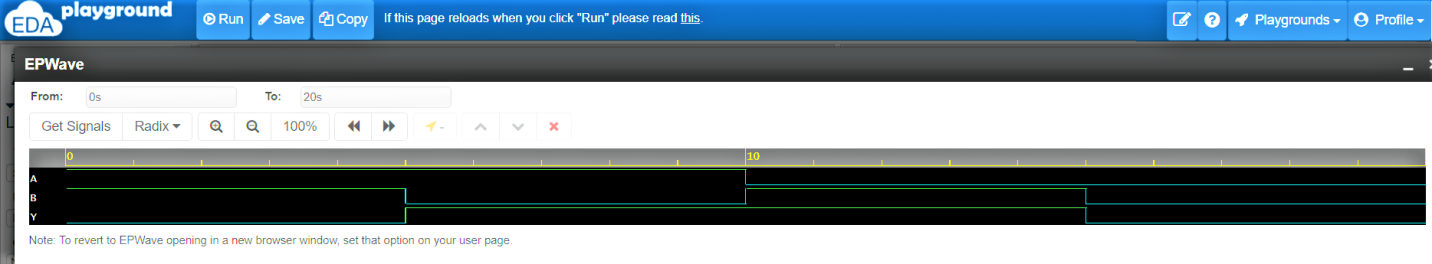
1. Representation of XOR gate using only NAND gates and perform the following operations:
   1. Derive the Boolean expression.
   2. Write the truth table for the above expression
   3. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?











**Design bench.sv**

module

gate1 (input a,b, output y);

assign y = ~(~(a&(~(a&b)))&~(b&~(a&b)));

endmodule

**Test bench.sv**

module tb\_gate();

reg A,B;

wire Y;

//print

//Ayushman Pranav E21cseu0245

gate1 a1(.a(A),.b(B),.y(Y));

initial begin

A=1;B=1;#5;

$display("A B Result");

$display("%b %b %b",A,B,Y);

A=1;B=0;#5;

$display("%b %b %b",A,B,Y);

A=0;B=1;#5;

$display("%b %b %b",A,B,Y);

A=0;B=0;#5;

$display("%b %b %b",A,B,Y);

end

// EP wave

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

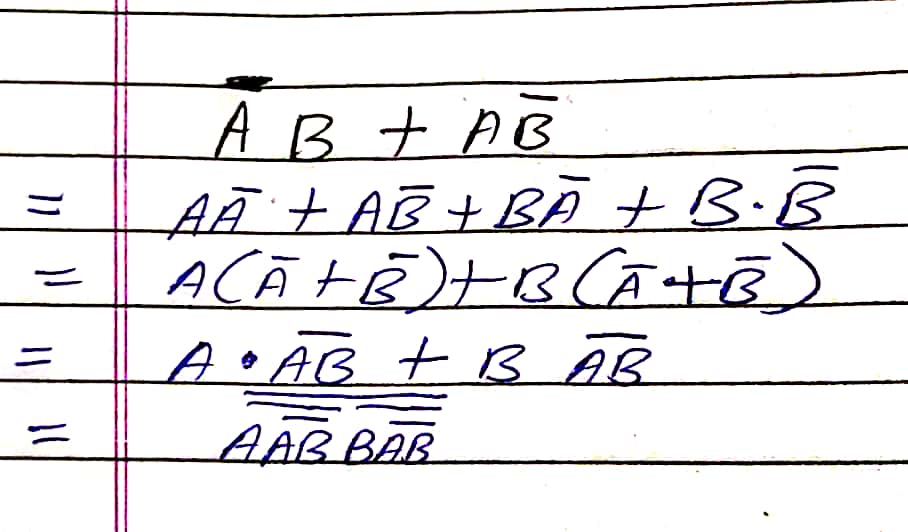
end

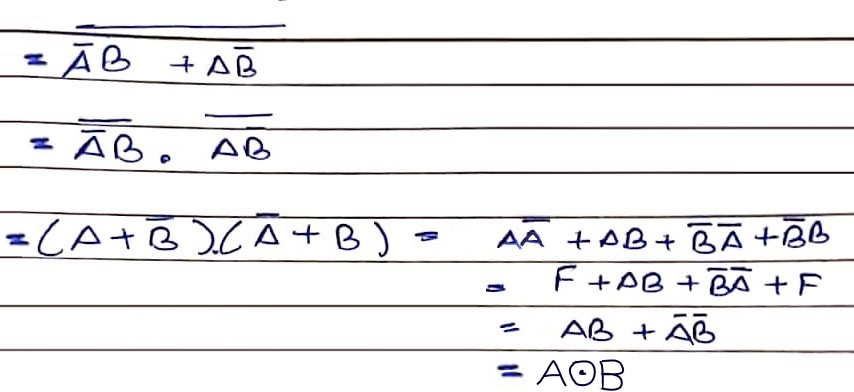
endmodule

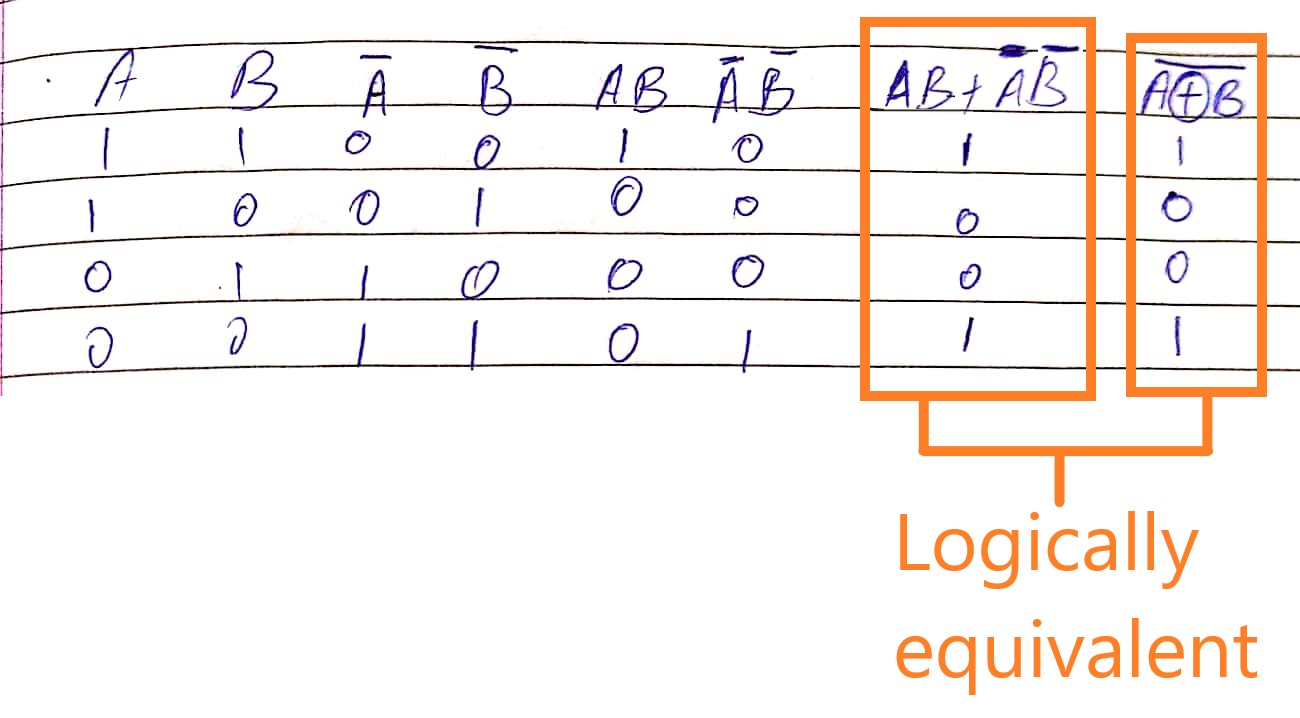
1. For the given circuit diagram do the following:
2. Derive the Boolean expression.
3. Write the truth table for the above expression
4. Write a Verilog code for each Boolean expression and then test using wave form and compare with truth table whether your circuit produced same output or not?

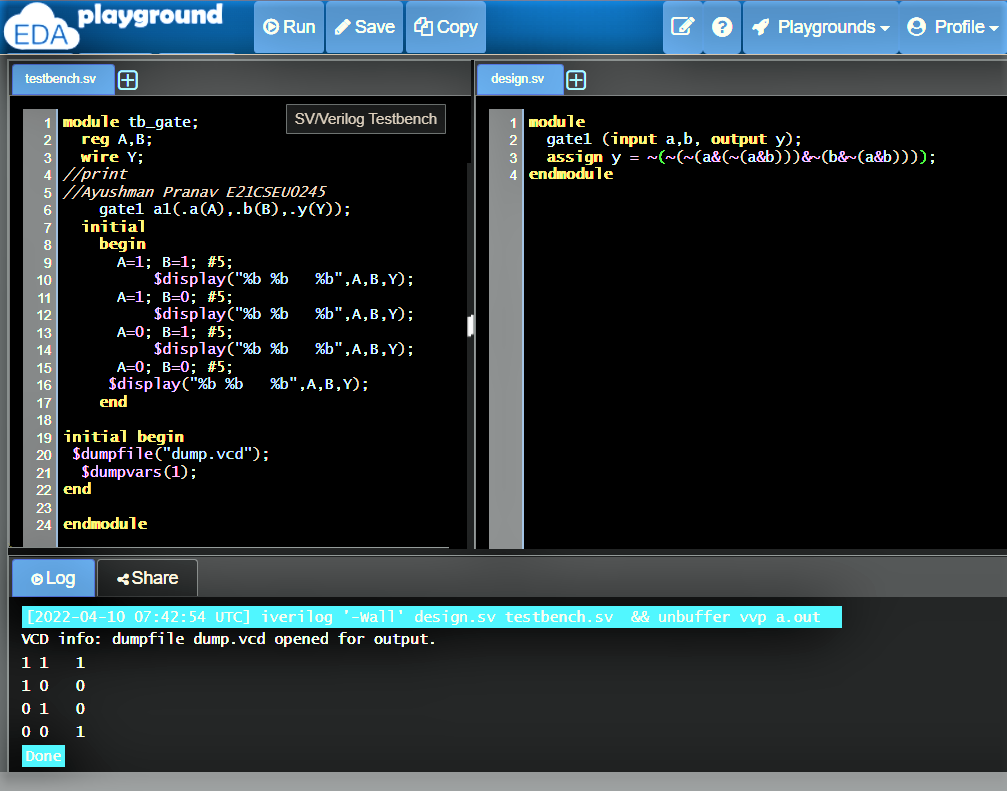
Diagram, schematic

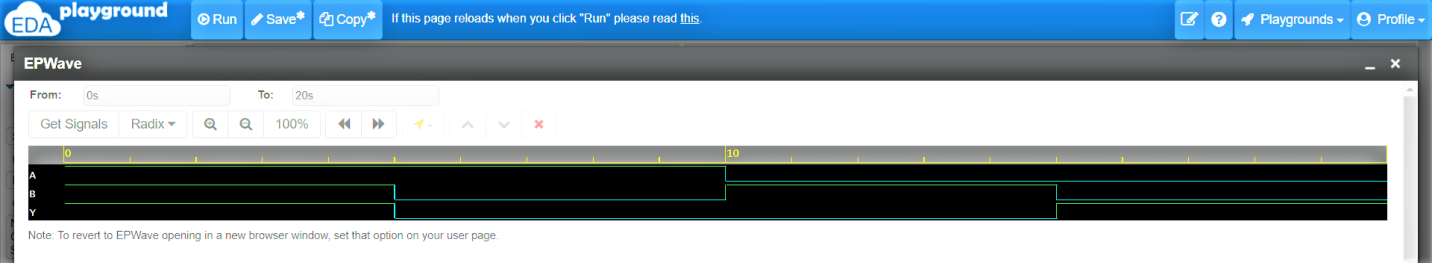
Description automatically generated











**Design bench.sv**

module

gate1 (input a,b, output y);

assign y = ~(~(~(a&(~(a&b)))&~(b&~(a&b))));

endmodule

**Test bench.sv**

module tb\_gate;

reg A,B;

wire Y;

//print

//Ayushman Pranav E21CSEU0245

gate1 a1(.a(A),.b(B),.y(Y));

initial

begin

A=1; B=1; #5;

$display("%b %b %b",A,B,Y);

A=1; B=0; #5;

$display("%b %b %b",A,B,Y);

A=0; B=1; #5;

$display("%b %b %b",A,B,Y);

A=0; B=0; #5;

$display("%b %b %b",A,B,Y);

end

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

end

endmodule